Technical Specification
IQ65033QTA14

36-75 V @ 14 A	3.3 V & 5.0 V	Quarter-brick ATCA
Input / Output	Management Power	Power Interface Module

The IQ65033QTA14 iQor Power Interface Module integrates all features required by the AdvancedTCA Base Specification into a Quarter-Brick footprint. The iQor offers industry leading external hold-up capacitor volumetric density for a compact overall solution. At 90 V hold-up capacitor voltage (trimmable 50-95 V), only 1.1 mF is required to achieve 8.7 ms hold-up time at 400 W. The -48 V output voltage is conditioned for smooth operation through severe input transient events. The iQor is designed thermally and electrically to drive higher power, wide-range-input, DC/DC converters such as the 480 W SynQor SQ60120QZB40 and 400 W SynQor PQ60120QZB33. RoHS Compliant (see last page).

IQ65033QTA14 Module

Operational Features

- Improved common-mode noise filtering
- Input ORing for A & B power feeds (MOSFET-based for low power dissipation)
- Hot swap control with seamless ride-through of input voltage transient
- EMI filter meets CISPR 22 Class B when used as directed (see applications section)
- External hold-up capacitor trimmable from 50-95 V
- Automatic discharge of external hold-up capacitor
- Isolated management power of 3.3 V at 3.6 A and 5.0 V at 150 mA
- Dual input side enable
- I^2C interface data reporting (optional)

Mechanical Features

- Industry standard quarter-brick size: 1.45" x 2.3" (36.8x58.4 mm)
- Overall height of 0.72" (18.2 mm), permits better airflow and smaller card pitch
- Total weight: 1.3 oz (38 g)
- Flanged pins designed to permit surface mount soldering (avoid wave solder) using FPiP technique
- External hold-up capacitor footprint much smaller than other solutions currently available on the market

Protection Features

- Management power over-voltage protection
- Management power over-current protection
- Main output over-current protection
- Thermal shutdown protects the unit from abnormal environmental conditions
- Input fuse/feed loss alarm
- Reverse voltage protection

Safety Features

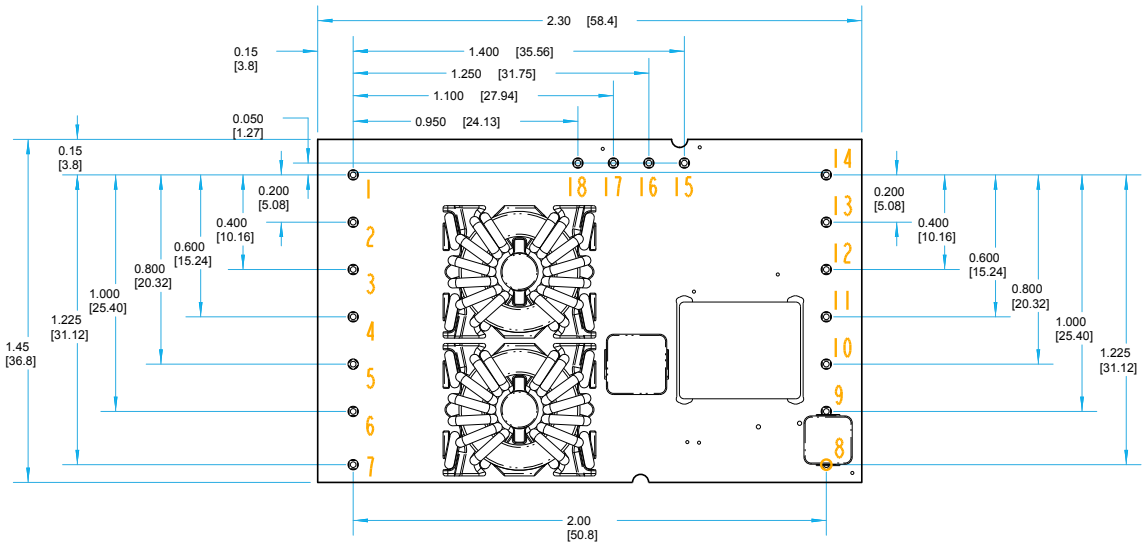
- 2250V, 30 MΩ VRTN_A/B to LOGIC_GND and SHELF_GND isolation
- UL 60950-1
- CAN/CSA-C22.2 No. 60950-1
- EN 60950-1

Contents

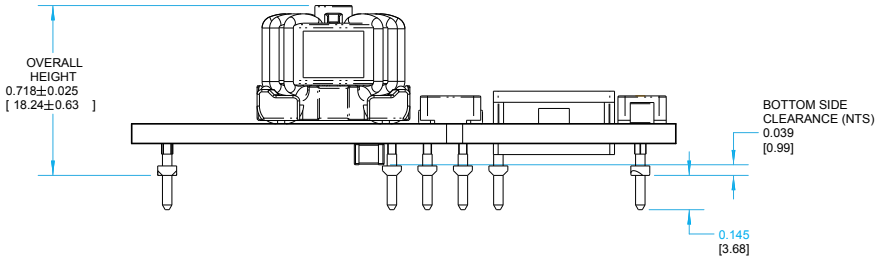
Mechanical Diagram

Input: 36-75 V
Outputs: 3.3 V & 5.0 V
Current: 14 A
Package: Quarter-brick

Top View



Side View



NOTES

1) All Pins are 0.040" (1.02 mm) diameter with 0.080" (2.03 mm) diameter standoff shoulders.
2) Other pin extension lengths available. Recommended pin length is 0.03" (0.76 mm) greater than the PCB thickness.
3) All Pins: Material - Copper Alloy
   Finish - Matte Tin over Nickel plate
4) Undimensioned components are shown for visual reference only.
5) All dimensions in inches
   Tolerances: x.xx +0.02"
   x.xxx +0.010"
6) Weight: 1.3 oz (38 g) typical
7) Workmanship: Meets or exceeds IPC-A-610C Class II
8) The flanged pins are designed to permit surface mount soldering (allowing to avoid the wave soldering process) through the use of the flanged pin-in-paste technique.

* Pins 10, 11, and 12 are only available on the full feature version. See the ordering page for more information.

** Single resistor connected externally to LOGIC_GND selects the three least significant bits of I2C Address "0101xxx".

PIN DESIGNATIONS

Pin No.	Name	Function
1	-48V_A	Negative A Feed (Externally Fused)
2	-48V_B	Negative B Feed (Externally Fused)
3	VRTN_A	Positive A Feed (Externally Fused)
4	VRTN_B	Positive B Feed (Externally Fused)
5	ENABLE_A	Enable A Input (Externally Fused)
		(Short Pin Tied to VRTN_A on Backplane)
6	ENABLE_B	Enable B Input (Externally Fused)
		(Short Pin Tied to VRTN_B on Backplane)
7	SHELF_GND	Shelf Ground
8	5.0V	5.0V (Relative to LOGIC_GND)
9	3.3V	3.3V (Relative to LOGIC_GND)
10	I2C_ADR	I2C Address Input *
		(Connect External Resistor to LOGIC_GND) **
11	I2C_DAT	I2C Data (Relative to LOGIC_GND) *
12	I2C_CLK	I2C Clock (Relative to LOGIC_GND) *
13	LOGIC_GND	Logic Ground
14	ALARM	Isolated A/B Feed Loss or Open Fuse Alarm
		(Relative to LOGIC_GND)
15	-48V_OUT	Negative Output to Payload Power Converter
16	HU_TRIM	Hold-Up Voltage Trim
		(Connect External Resistor to -48V_OUT)
17	VRTN_OUT	Positive Output to Payload Power Converter
18	HU_CAP	Positive Connection to Hold-Up Capacitor
		(Negative Connection to -48V_OUT)

IQ65033QTA14 Electrical Characteristics

Specifications subject to change without notice. Specifications in **BOLD** apply over the temperature range -40 ºC to 100 ºC.

Parameter	Min.	Typ.	Max.	Units	Notes & Conditions
ABSOLUTE MAXIMUM RATINGS					
Input Voltage					-48V_A/B & ENABLE_A/B
Continuous			-75	V	Limited by internal TVS zener diode
Transient			-100	V	1 ms transient, square wave
Reverse Polarity			+75	V	No damage, low current
Isolation Voltage					
(VRTN_A/B to LOGIC_GND)			2250	V	
(VRTN_A/B to SHELF_GND)			2250	V	
-48 V Output	+1		-95	V	At -48V_OUT w.r.t. VRTN_OUT; limited by TVS diode
3.3 V Management Power Output	-0.5		4.5	V	5.5 V transient for 1 s
5.0 V Management Power Output	-0.5		9	V	
Hold-up Capacitor Voltage					Relative to -48V_OUT
Enabled - Continuous			100	V	150 V transient, 1 ms
Disabled - Continuous			18	V	Limited by self-heating of holdup discharge circuit
I2C_ADR,DAT,CLK Pins	-0.5		4.5	V	Not to exceed 3.3 Vout + 0.3 V
ALARM Pin	-1		40	V	Not to exceed 200 mA
Operating Temperature	-40		100	°C	Subject to thermal derating; see Figures 1 & 3
Storage Temperature	-55		125	°C	
-48 V DUAL FEED INPUT CHARACTERISTICS					
Input Voltage Range	-36	-48	-75	V	Subject to the Threshold Protocol used
Operating Current			14	A	25 ºC, 200 LFM; see Figure 1
Disabled Input Current		7.5	**10**	mA	Vin = -32 V
Enabled No-Load Input Current		25	40	mA	Vin = -48 V
Internal Input Filter Capacitance (Not Hot-Swapped)		20	26	µF	Should be precharged by resistors to EARLY_A/B pins
Recommended EARLY_A/B Resistors	37	100	120	Ω	2010 case size KOA SG73 or equivalent; see Note 8
Recommended Input Fuses			17	A	
3.3 V ISOLATED MANAGEMENT POWER					
Startup Delay					Time from ENABLE_A/B to 3.3/5.0 Vout
At -36 Vin		380	**470**	ms	
At -48 Vin		210		ms	
At -75 Vin	**50**	120		ms	
Turn-On Rise Time	1	5	20	ms	0% to 90%; see Figure 6
Input Under-Voltage Lockout (UVLO)					At Mangement Power Converter input; See Figure A
Turn-On Voltage Threshold (-E Threshold)	**-25.5**	-26.5	**-28.0**	V	Subject to ENABLE_A/B pin status; see Note 3
Turn-Off Voltage Threshold (-E Threshold)	**-24.0**	-26.0	**-27.5**	V	Subject to ENABLE_A/B after 100 ms delay; Note 3
Total Output Voltage Range	**3.100**	3.350	**3.450**	V	Including line, load, sample, life, and temp
Output Voltage Ripple and Noise					See Figure 12
Peak-to-Peak		75	140	mV	Full load, 10 µF ceramic, 20 MHz bandwidth
RMS		25	50	mV	Full load, 10 µF ceramic, 20 MHz bandwidth
Operating Output Current Range	0		3.6	A	Subject to thermal derating; see Figures 1 & 3
Output DC Current-Limit Inception	**3.9**	5.4	**6.9**	A	Vout = 90%, Varies with Vin
Current Limit Shutdown Voltage		1.5		V	Initiates hiccup mode
Hiccup Mode Restart Time		130		ms	Vin = -48 V
Back-Drive Current			55	mA	Negative current drawn from output source; 3.6 V
Maximum Output Capacitance			1000	µF	
Switching Frequency	200	220	240	kHz	Management power converter
Over-Voltage Protection Inception	**3.70**	4.00	**4.25**	V	
5.0 V POWER (Derived From 3.3 V Converter)					
Total Output Voltage Range	**4.80**	5.00	**5.20**	V	Including line, load, sample, life, and temp
Operating Output Current Range	0		150	mA	
Short Circuit Current		400		mA	Independent Thermal Protection
Back-Drive Current			1	mA	Negative current drawn from output source
Maximum Output Capacitance			1000	µF	

IQ65033QTA14 Electrical Characteristics (continued)

Specifications subject to change without notice. Specifications in **BOLD** apply over the temperature range -40 ºC to 100 ºC.

Parameter	Min.	Typ.	Max.	Units	Notes & Conditions
DUAL ENABLE INPUT CHARACTERISTICS					
ENABLE_A/B Threshold					
-E Threshold Protocol	**-32.0**	-34.0	**-35.8**	V	At input feed voltage -48V_A/B; see Figure A
Current Drain per Enable Pin			**0.38**	mA	Vin = -75 V
-48V OUTPUT					
Efficiency					No load on 3.3/5.0 V outputs, Vin = -48 V
500 W Output Power	98.3	98.9		%	
350 W Output Power	98.6	99.0		%	
Equivalent Resistance from Input Feed		35	**65**	mΩ	Load ≥ 2 A
Recommended External Output Filter Capacitance	80	100	330	µF	Load during startup ≤ 100 mA; see Notes 1 & 7
Hot-Swap Startup Ramp dV/dt	**180**	230	**280**	V/s	Constant for all input voltages
Output Voltage Delay		420	**650**	ms	Varies inversely with Vin; see Note 6 & Figure 7
Output Current Limit	36	40	46	A	Hold-up remains active
Input dV/dt Limit (Turns Off Hot-Swap Momentarily)		55		V/ms	Hold-up remains active
Short Circuit Duration to Initiate Hiccup Mode		2		ms	
Restart Time Hiccup Mode	**1.8**	2.0	**2.2**	s	
INPUT ORING					
ORing MOSFET Turn On Current	**0.5**	1.2	**1.9**	A	
ORing MOSFET Turn Off Current	**0.1**	0.7	**1.3**	A	
ORing MOSFET Current Hysteresis	**0.4**	0.5	**0.6**	A	
Turn-On Time		600		µs	
Turn-Off Time		0.2		µs	
HOLD-UP CAPACITOR INTERFACE					
Hold-up Capacitor Trim Range	50	90	95	V	Can be set either above or below input voltage
Hold-up Capacitor Charge Accuracy	**87.2**	90.0	**95.0**	V	2.49 kΩ external trim resistor; 1%, 100 ppm/ºC
External Hold-up Voltage Trim Resistor Power Dissipation			160	µW	
Hold-up Capacitor Charge Current		60		mA	
Switching Frequency	**405**	450	**495**	KHz	Hold-up power converter
-48V_OUT Threshold					See Note 2
To Arm Hold-up Connect (-E Threshold)	**-33.0**	-35.0	**-37.0**	V	At -48V_OUT w.r.t. VRTN_OUT; see Figure A
To Initiate Hold-up Connect (-E Threshold)	**-32.2**	-34.2	**-36.0**	V	At -48V_OUT w.r.t. VRTN_OUT; see Figure A
dV/dt on Hold-up Connect		90		V/ms	
Duration of Hold-up Connect		0.1		s	See Note 4
Delay Before Hold-up Connect is (Re)Armed		2		s	-48V output still enabled
Hold-up Capacitor Discharge Resistance	**560**	600	**640**	Ω	Discharges holdup to ≤ 60 V & 6 J within 1 second
Maximum Hold-up Capacitance			3300	µF	Yields 27 ms (400 W at 90 V cap charge)
Load Power During Hold-up Event			500	W	-48V Output
ISOLATED ALARM OUTPUT (ALARM = HI-Z)NOTE 5					
Input A/B Feed Voltage Alarm Threshold	**-36.4**	-38.4	**-40.4**	V	At input feed voltage -48V_A/B; see Figure A
Open Circuit Voltage			40	V	
On-State Voltage		0.2	**0.4**	V	At 50 mA
On-State Transistor Collector Current		50		mA	
Off-State Transistor Collector Current		1		µA	

Note 1: Total load on -48V output (including C_{filter} charging current) not to exceed 180 mA during hotswap ramp. See Figure D. $Load_{total}$ = Preload + 240·C_{filter}

Note 2: Hold-up operation with Vin below -43 V not required by ATCA specification.

Note 3: For most applications, the ENABLE_A/B lines will be tied to the input pins. When this is the case, management power undervoltage thresholds will be determined by ENABLE_A/B thresholds. Management power will continue to run for up to 100 ms after ENABLE_A/B falls below the turn-off threshold.

Note 4: -48V output does not recover after hold-up event unless input is above Arm Hold-up threshold.

Note 5: Does not inhibit -48V output and is non-latching.

Note 6: Full load can be applied to -48V output 650 ms after enable or 350 ms after the 3.3 V management power is running.

Note 7: For applications using semi or unregulated (BusQor) converters, any capacitance at the output of the unregulated converter (divided by the square of the converter turns ratio) shall be considered to also be present at the output of the ATCA module. For example, if there is 180 µF ±20% at the output of the ATCA module and 560 µF ±20% at the output of an SQ60120QZB40 (4:1 ratio), then the apparent ATCA output filter capacitance is 180 + 560/4^2 µF = 215 µF ±20%.

Note 8: Any resistor value may be used, but resulting system may not meet ATCA inrush requirements for all conditions. See Application Section for additional info.

IQ65033QTA14 Electrical Characteristics (continued)

Specifications subject to change without notice. Specifications in **BOLD** apply over the temperature range -40 ºC to 100 ºC.

Parameter	Min.	Typ.	Max.	Units	Notes & Conditions
I²C DATA REPORTING INTERFACE					
Maximum Clock Rate		100	400	kHz	Clock stretching occurs at the maximum rate
Measurement Error					
Feed Voltage A/B			**± 3+1**	% + LSB	Measurement may saturate outside -5 V to -75 V
Holdup Voltage			**± 3+1**	% + LSB	Measurement may saturate below 5 V
-48V_OUT Current			**± 3+1**	% + LSB	Measurement may saturate above 17.5 A
Temperature			**± 3**	°C	
OVER-TEMPERATURE PROTECTION					
Shutdown Point		135		°C	
Restart Hysteresis		10		°C	Automatic restart
RELIABILITY CHARACTERISTICS					
Calculated MTBF (Telcordia)		4.2		10^6 Hrs	TR-NWT-000332; 80% load, 300 LFM, 40 °C Ta
Calculated MTBF (MIL-217)		1.9		10^6 Hrs	MIL-HDBK-217F; 80% load, 300 LFM, 40 °C Ta
Field Demonstrated MTBF					See website for details
TEMPERATURE LIMITS FOR POWER DERATING CURVES					
Semiconductor Junction Temperature			125	°C	Package rated to 150 °C
Board Temperature			125	°C	UL rated max operating temp 130 °C
Transformer Temperature			125	°C	See Figure 3 for derating curve
Common-Mode Choke Temperature			125	°C	Curie temp 135 °C; rated for 200 °C operation

Parameter	Notes & Conditions
STANDARDS COMPLIANCE	
UL 60950-1	Basic insulation
EN 60950-1	
CAN/CSA-C22.2 No. 60950-1	

Note: An external input fuse must always be used to meet these safety requirements. Contact SynQor for official safety certificates on new releases or download from the SynQor website.

Parameter	# Units	Test Conditions
QUALIFICATION TESTING		
Life Test	32	95% rated Vin and load, units at derating point, 1000 hours
Vibration	5	10-55 Hz sweep, 0.060" total excursion, 1 min./sweep, 120 sweeps for 3 axis
Mechanical Shock	5	100g minimum, 2 drops in x, y and z axis
Temperature Cycling	10	-40 °C to 100 °C, unit temp. ramp 15 °C/min., 500 cycles
Power/Thermal Cycling	5	Toperating = min to max, Vin = min to max, full load, 100 cycles
Design Marginality	5	Tmin-10 °C to Tmax+10 °C, 5 °C steps, Vin = min to max, 0-105% load
Humidity	5	85 °C, 95% RH, 1000 hours, continuous Vin applied except 5 min/day
Solderability	15 pins	MIL-STD-883, method 2003

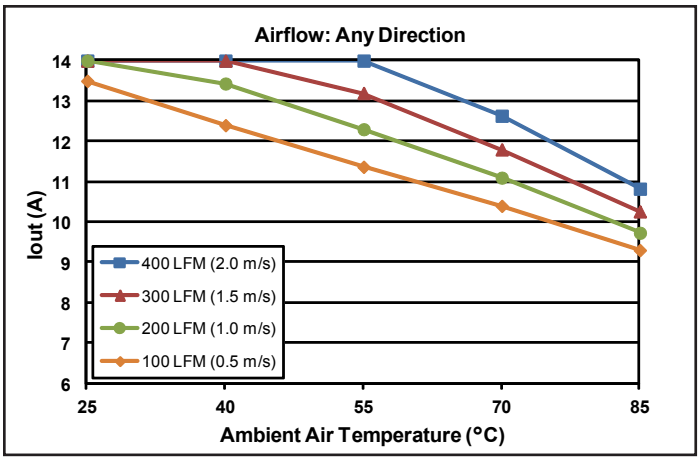


Figure 1: Derating Curves *(output current vs. ambient air temperature) with 3.3 V output at 1.5 A. Derating is applicable to all input voltages and airflow directions; however, optimal airflow is lengthwise (pin 14 ↔ pin 1). Pins 1,2,3,4,15,17 soldered to copper planes with solder fillets on both sides.*

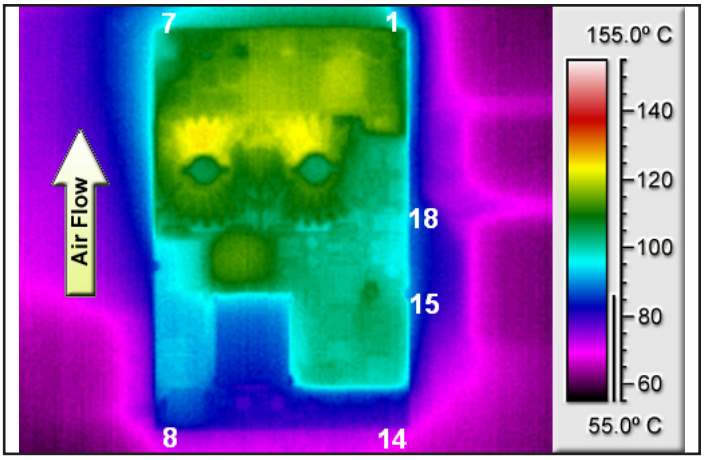


Figure 2: Thermal Image *of module at 12.3 A load current from -48V output, with 55 °C air flowing at the rate of 200 LFM, and the 3.3 V output at 1.5 A. Air is flowing across the module from pin 14 → pin 1. Pins 1,2,3,4,15,17 soldered to copper planes. Module oriented on end.*

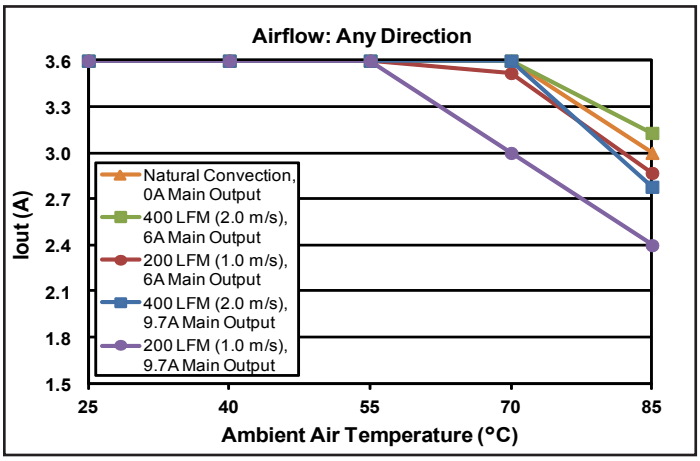


Figure 3: 3.3V Derating Curves *(output current vs. ambient air temperature) with -48 V output at various load currents and wind speeds. Pins 1,2,3,4,15,17 soldered to copper planes with solder fillets on both sides. Derating is applicable to all input voltages and airflow directions.*

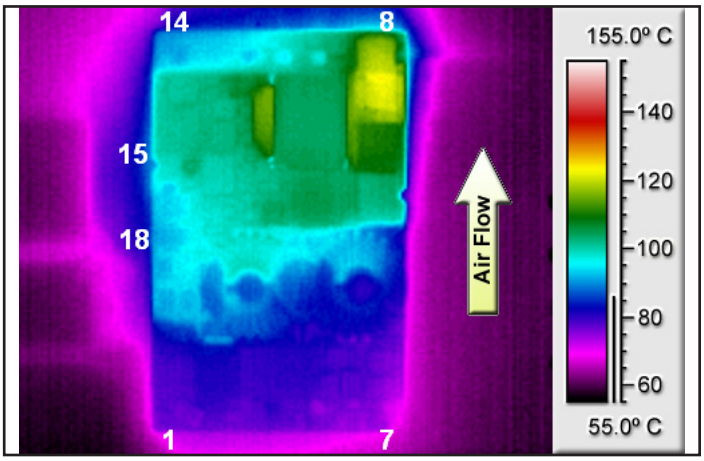


Figure 4: Thermal Image *of module at 3.6 A load current from 3.3 V output with 55 °C air flowing at the rate of 200 LFM. Air is flowing across the module from pin 1 → pin 14 (-48 Vin, -48 V output at 9.7 A). Pins 1,2,3,4,15,17 soldered to copper planes. Module oriented on end.*

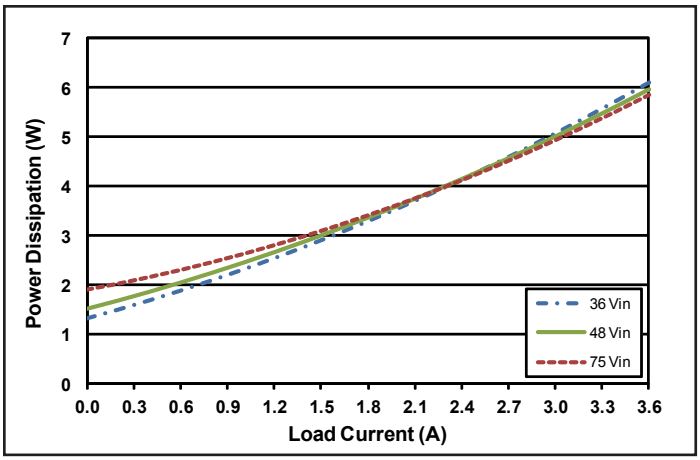


Figure 5: 3.3V Power Dissipation *vs. 3.3 V Management Power load current.*

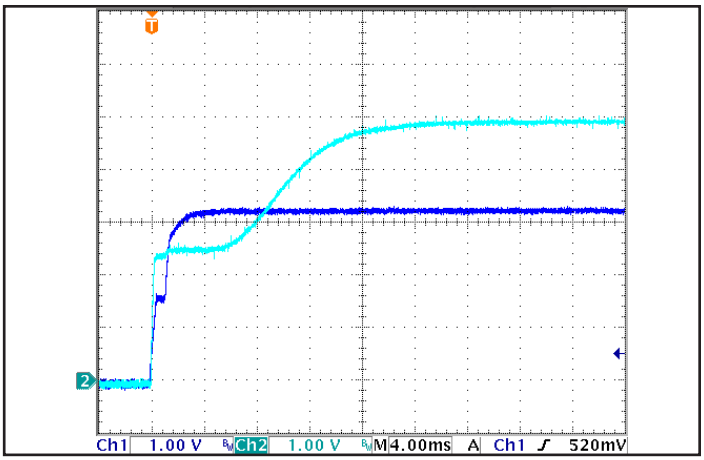


Figure 6: Management Power Turn-on Transient *at 50% load (4 ms/div). Load capacitance: 10 µF ceramic capacitor. Ch 1: 3.3 Vout (1 V/div). Ch 2: 5.0 Vout (1 V/div).*

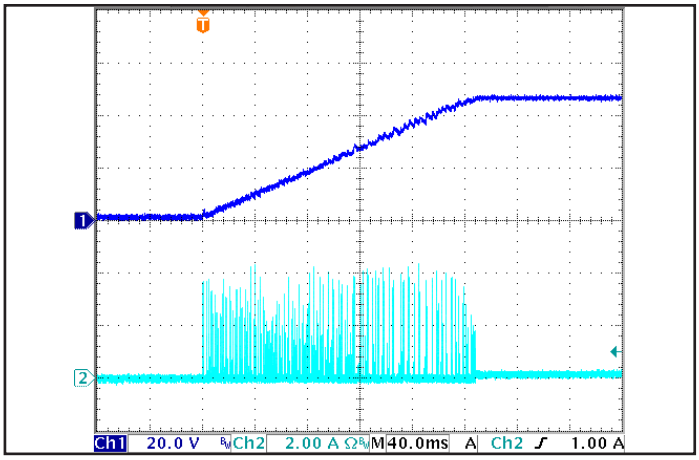


Figure 7: 48 V Hot-Swap Turn-on Transient *(220 µF electrolytic output filter capacitor C_p 100 mA preload). Top trace: VRTN_OUT w.r.t. -48V_OUT (20 V/ div), Bottom trace: Input Feed Current (2 A/div).*

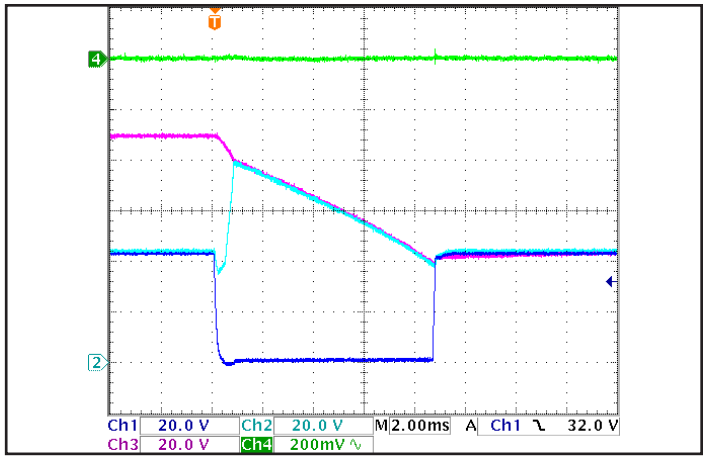


Figure 8: 8.70 ms Zero Volt Transient *(1200 µF electrolytic hold-up capacitor CH, 100 µF electrolytic output filter capacitor C_p). 400 W load. Ch 1: Input Feed A/B Voltage (20 V/div). Ch 2: VRTN_OUT w.r.t. -48V_OUT (20 V/div). Ch 3: HU_CAP w.r.t. -48V_OUT (20 V/div). Ch 4: 3.3V_OUT (200 mV/div).*

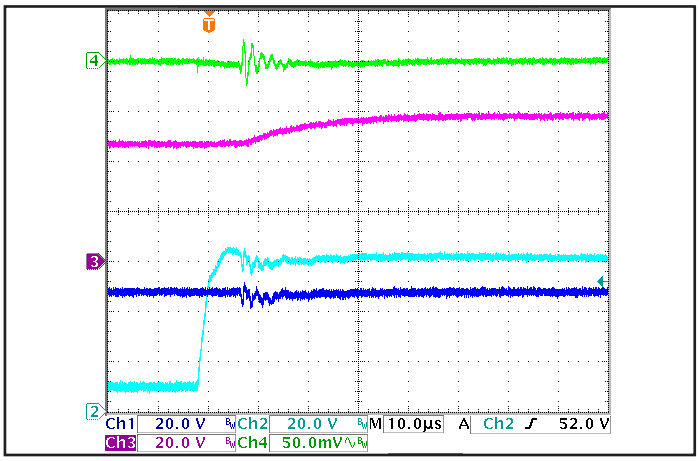


Figure 9: Instantaneous Input Transient *from 48 V Feed A to 60 V Feed B. Ch 1: Input Feed A Voltage (20 V/div). Ch 2: Input Feed B Voltage (20 V/ div). Ch 3: VRTN_OUT w.r.t. -48V_OUT (20 V/div). Ch 4: 3.3V_OUT (50 mV/div).*

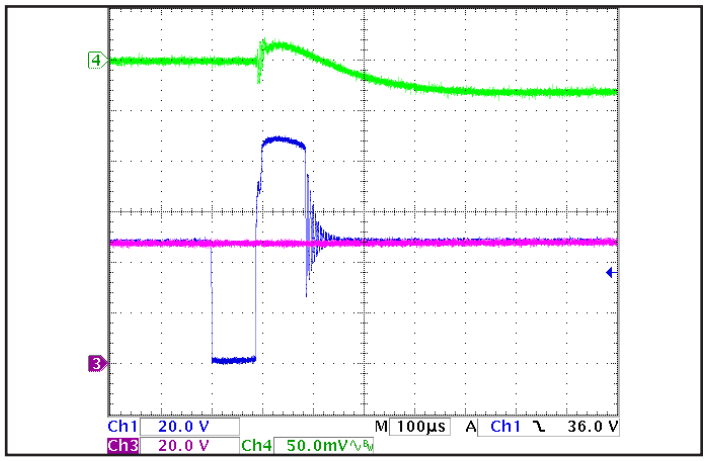


Figure 10: Inductive Switching Event *on Feed A from 48 V to 0 V to TVS Zener clamping voltage. No load on -48V output. Ch1: Input Feed A Voltage (20 V/div). Ch3: VRTN_OUT w.r.t. -48V_OUT (20 V/div). Ch 4: 3.3V_OUT (50 mV/div).*

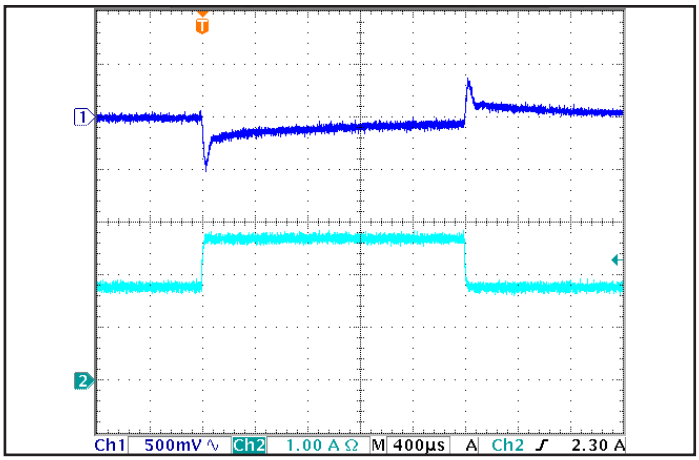


Figure 11: 3.3 Vout Response to a Step-change in Load Current *[50%-75%-50% of Iout(max): dI/dt = 1 A/µs]. Load capacitance: 10 µF ceramic capacitor. Top trace: 3.3 Vout (500 mV/div). Bottom trace: Iout (1 A/ div).*

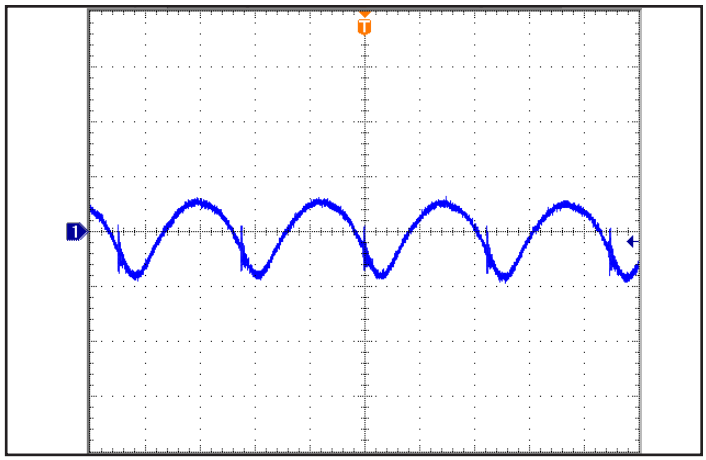


Figure 12: 3.3 Vout Ripple *at nominal input voltage at rated load current (50 mV/div). Load capacitance: 10 µF ceramic capacitor. Bandwidth: 20 MHz.*

FEATURE DESCRIPTIONS

Input ORing MOSFETs: ORing of dual -48V feeds is provided by four MOSFETs, which are individually controlled so as to operate as an ideal diode (see Figure A). If there is an input feed short of any kind, a control circuit will detect reverse current and turn off the MOSFET in 250 ns (typ.), to avoid disturbing the other feed voltage. At zero current, the MOSFET is guaranteed to be off. In the case of a fuse failure, this triggers the ALARM output, due to an apparent input feed loss. Current hysteresis prevents limit cycling around the transition point between body diode and MOSFET conduction. Due to the 'Turn On Current' feature, at fixed input voltages the output voltage will experience one or two diode drops (0.6 V or 1.2 V) for currents at or below 'Turn On Current' thresholds.

ALARM Output: The ALARM pin gives an external indication of a fault condition. It is an isolated and buffered open-collector output, which is normally pulled low. In the presence of an input feed loss (which can be caused by a fuse failure), the ALARM output will be tri-stated.

External Input Fuse Failure Detection: At zero current, the input ORing MOSFETs are guaranteed to be off. In the case of a fuse failure, an on-board bleed resistor pulls the input feed voltage down. This triggers the ALARM output due to an apparent input feed loss. There are two main downsides to this approach. First, there is no way to distinguish between a feed loss and a fuse failure. Second, an enable fuse loss is not detected, since the enables are diode OR'd.

The full featured version of the iQor offers additional data reporting that makes full fuse detection possible. Among other data, each feed voltage and each enable voltage is reported through the I²C port. These voltages can be compared with the voltages reported by the shelf manager to determine whether any board fuse is blown.

Input Enable: The ENABLE_A/B signals connect to VRTN_A/B on the backplane via the shortest pins in the zone 1 connector. They are the last pins to mate during board insertion, and the first to disconnect during board extraction. The ENABLE_A and ENABLE_B signals are diode-ORed together which lets either signal enable the module. Whenever both ENABLE pins are open, the hot-swap switch is opened. This prevents -48V output power from being drawn though the EARLY pre-charge resistors.

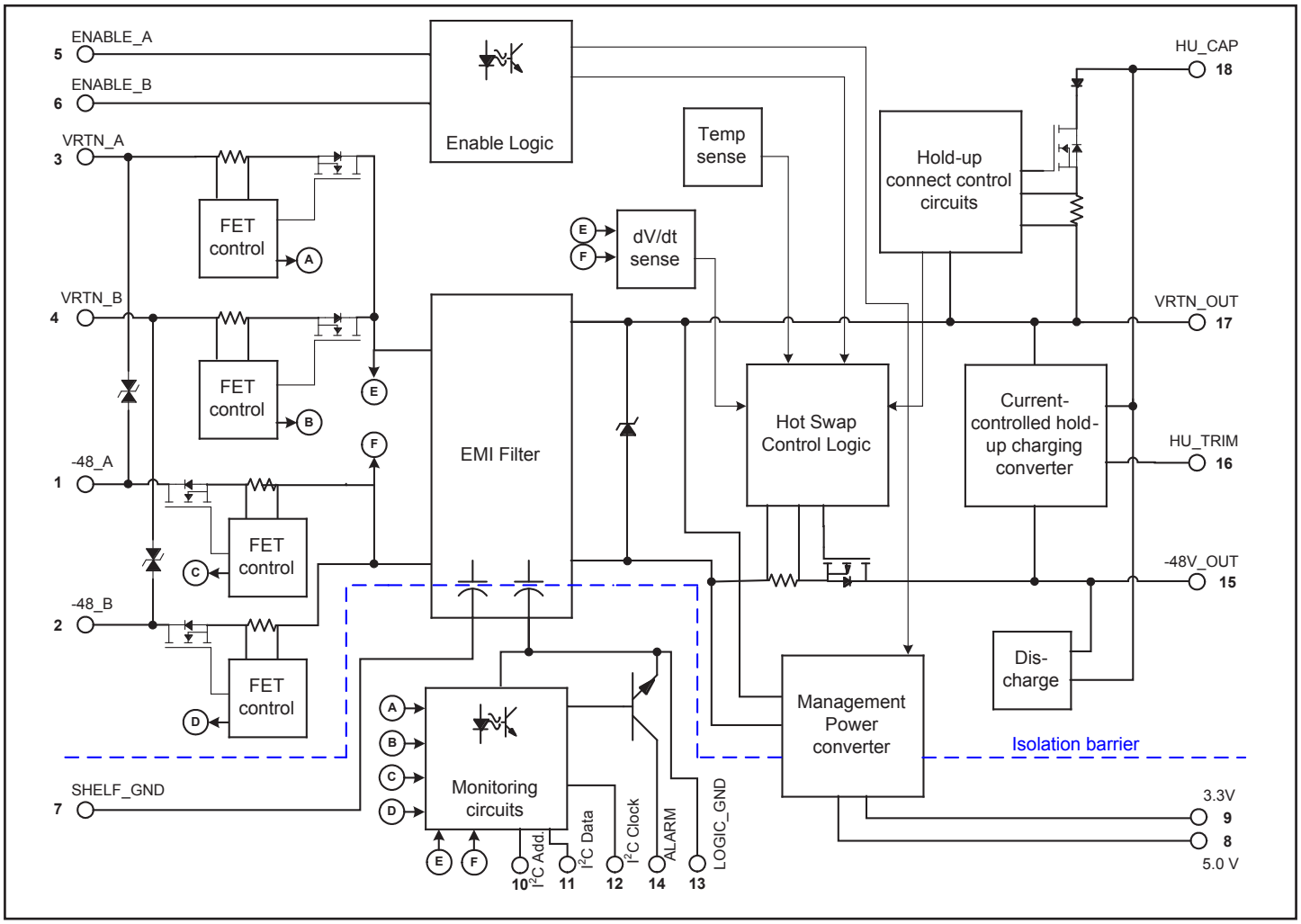


Figure A: Internal Block Diagram

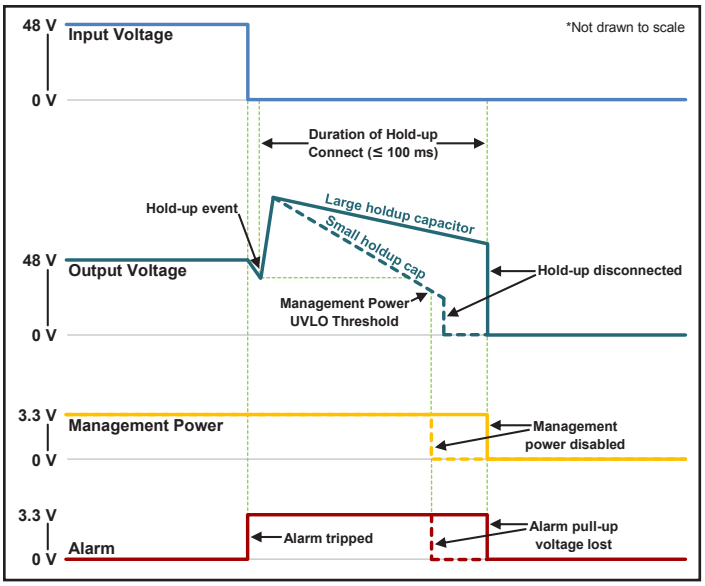


Figure B: *Sudden Loss of Input Power*

The ENABLE signals also control the management power. Upon board insertion, the management power remains off until at least one of ENABLE_A/B is connected. Upon board extraction, the management power is disabled at the end of the 100 ms hold-up period, and remains off until ENABLE_A/B is reconnected. This prevents the IPMI controller from reading an invalid hardware address when a board is partially inserted. Management power flows through the EARLY pre-charge resistors for a maximum of 100 ms, which provides a margin similar to the pre-charge event in terms of resistor safe-operating-area.

EARLY Precharge Resistors: The EARLY_A/B signals connect to the longest pins in the zone 1 power connector, and therefore first to mate during board insertion. External resistors connected between these signals and -48V (A and B) allow the relatively small EMI filter capacitance to be precharged before the main power pins make contact. Worst-case peak power requirement is $(Vin_{max} - 32)^2/R$ for 100 ms. SynQor recommends using one (1x) 2010 case size KOA/Speer SG73 series, two (2x) 0805 case size Panasonic ERJ-P6W series, or equivalent surge-rated resistors.

Hot Swap - Thermal Shutdown: To protect the unit from damage in an abnormal thermal environment, the hot-swap switch will be disabled when the thermal sensor temperature rises above the turn-off threshold. The switch will be automatically enabled again when the temperature goes below the turn-on threshold. The management power remains on during an over-temperature condition.

The full featured version of the iQor reports the actual temperature through the I^2C port.

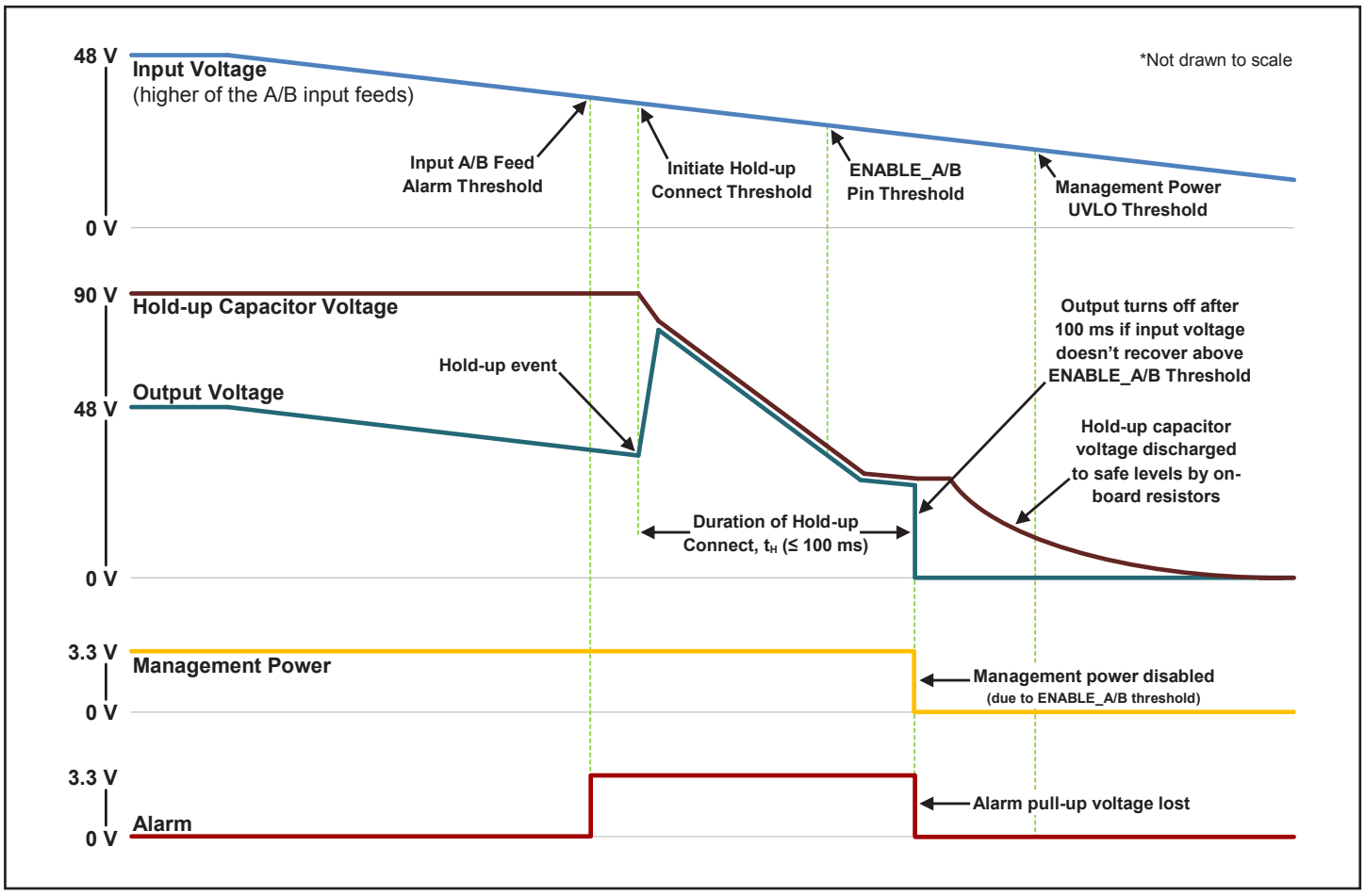


Figure C: *Gradual Loss of Input Power*

Hot Swap - Over-Current Protection: If the -48V output current rises above the current limit threshold, the hot-swap switch will be disabled, and will immediately enter another soft-start sequence. If an output short is detected, the hot-swap switch will be disabled and will enter a hiccup mode of operation with automatic restart.

The full featured version of the iQor reports actual output current through the I²C port.

Hot Swap - Transient Suppression: Input transient events can occur if there is a short on an adjacent board or backplane. The short builds up a large current in the wiring inductance, and when a fuse blows, the voltage behind the fuse spikes very quickly. This can cause a loss of redundancy since many other boards could be exposed to this spike.

The iQor unit conditions the -48V output, providing for seamless ride-through of input voltage transients. If the positive dV/dt of the input voltage is too high, the hot-swap switch will be disabled and will immediately enter another soft-start sequence. This limits the dV/dt seen on the -48V output, which prevents the 12V payload power converter from having such a large glitch on its output that it shuts down. The -48V output hold-up function remains active throughout, in case the hot-swap switch is forced off for too long.

Passive Transient Suppression: Each input feed has a dedicated internal bidirectional TVS zener diode, rated for a minimum clamp voltage of 77.8V at 1mA. A TVS diode short due to electrical overstress will not disable the iQor module: a fuse will open, and the module can continue to run from the other feed.

External Hold-up Capacitor Charge: A current controlled DC-DC converter charges the external hold-up capacitor to a voltage of 50-95 V, set by an external resistor. The charge voltage can range either above or below the input feed voltage. Constant current charging takes place whenever the hot-swap switch is enabled.

Hold-up Capacitor Connect: When the hot-swap switch is enabled, 2 seconds are allocated to charge the hold-up capacitor. After this time, a comparator is armed, which connects the hold-up capacitor to the -48V output should the output ever drop below the given connect threshold. A current limit circuit protects against damage during a short circuit condition. A dV/dt limit circuit regulates the hold-up connect switch turn-on speed. When the comparator is tripped, the hold-up connect switch remains closed for 100 ms, is off for 2 seconds to allow the hold-up capacitor to recharge, and then is automatically rearmed (if the output voltage is above the given arm threshold).

Hold-up Capacitor Discharge: Whenever the hot-swap switch is disabled, an internal resistor bank is connected across the hold-up capacitor. This is intended to quickly reduce the voltage and energy on the hold-up capacitor to safe levels.

Management Power: An isolated management power converter delivers both 3.3 V and a low power 5.0 V relative to LOGIC_GND. Overcurrent protection operates in constant current with a hiccup mode if the output voltage drops too far. Output over-voltage circuitry is included with a redundant reference and optocoupler.

The events from power up to availability of output voltage and full payload current are illustrated in the timing diagram shown in Figure D.

Hot Swap – Shutdown Timing: In the event of a sudden loss of input voltage (see Figure B), a hold-up event will be triggered. When the output voltage (plus a diode drop for the hot-swap body diode) decays to the management power under-voltage turn-off threshold the 3.3V/5.0V outputs will shut down and the main -48V output will disconnect from the hold-up shortly thereafter.

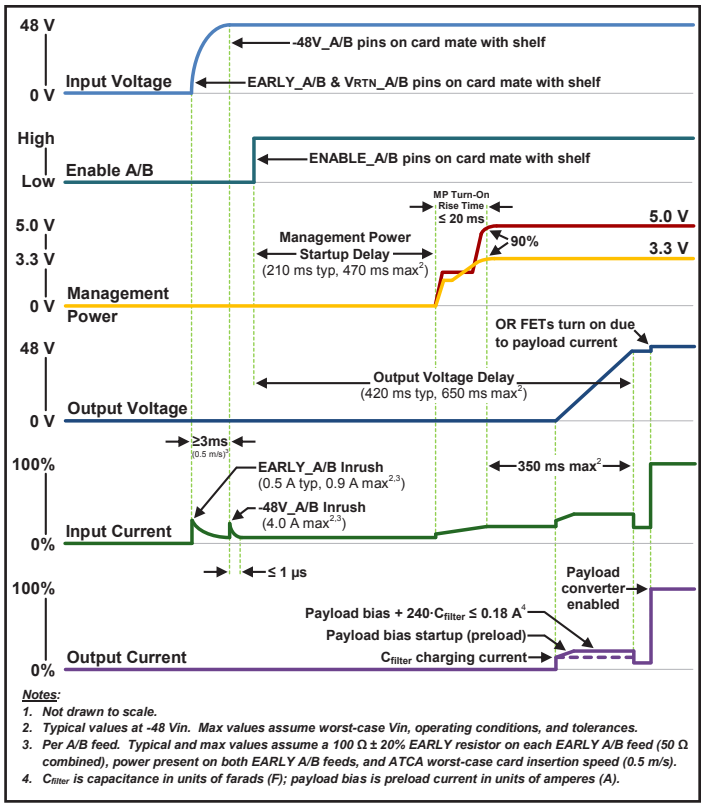


Figure D: *Power-up (board insertion) Timing Diagram*

In the event of a gradual loss of input voltage (Fig. C), the main -48V output will shut down 100 ms after the beginning of the hold-up event. The -48V output will enter a hiccup mode of operation for input voltages below the Hold-up Arm Threshold. Management power will continue to run until the input voltage (plus 0 V to 1.2 V for the ORing MOSFETs) decays to the management power under-voltage turn-off threshold or ENABLE_A/B decays to below its turn-off threshold, whichever comes first.

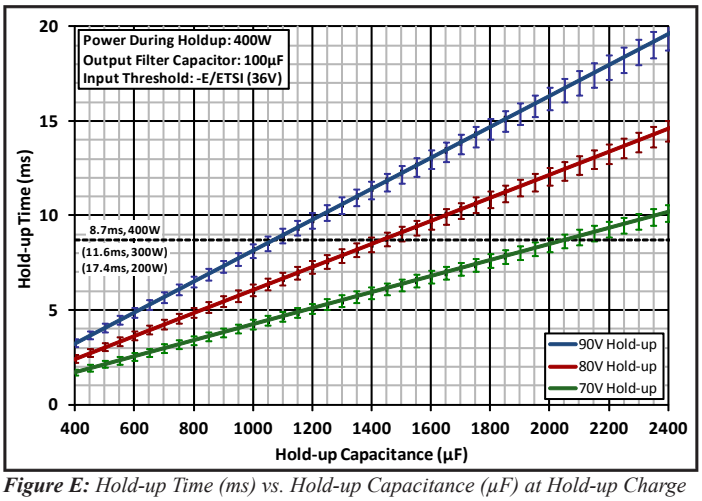


Figure E: *Hold-up Time (ms) vs. Hold-up Capacitance (µF) at Hold-up Charge Voltages of 70 V, 80 V, and 90 V (see Equation A). The AdvancedTCA hold-up time requirement is at most 8.70 ms (dashed horizontal line). The capacitor tolerance is not factored into this result. Error bars indicate the worst case range of hold-up time for a given hold-up capacitance.*

EXTERNAL HOLD-UP CAPACITOR SELECTION

C_H is the hold-up capacitance (electrolytic capacitors typically have a ±20% tolerance):

$$C_H = \frac{2t_H P_H}{(V_H - 1.5)^2 - (V_U)^2} \qquad \textit{Equation A}$$

Typically a strong function of V_H (see Figure E).

Where:

V_H = hold-up capacitor charge voltage.

V_U = minimum operating voltage on the -48V output; the greater of the under-voltage lockout threshold of the payload power converter, and the under-voltage lockout threshold of the management power converter.

t_H = time from when the highest input feed voltage drops below V_F, to the time when the highest input feed voltage rises above V_U. The ATCA specification requirement is 8.70 ms (see Figure F).

V_F = voltage at which the hold-up capacitor is engaged.

P_H = power drawn from the hold-up capacitor, the sum of the input power of the payload power converter and the input power of the 3.3 V management power converter (see Figure 5):

$$P_H = \frac{P_{OUT\,12V}}{\eta_{12V}} + P_{OUT\,3.3V} + P_{D\,3.3V} \qquad \textit{Equation B}$$

Where:

$P_{OUT\,12V}$ = output power delivered by the payload power converter.

η_{12V} = efficiency of the payload power converter.

$P_{OUT\,3.3V}$ = output power delivered by the 3.3 V management power converter.

$P_{D\,3.3V}$ = power dissipated in the 3.3 V management power converter (see Figure 5).

EXTERNAL HOLD-UP CAPACITOR VOLTAGE RATING

Operating electrolytic capacitors near their voltage rating does not significantly affect their reliability, as it does with tantalum or ceramic type capacitors. The operating life of electrolytic capacitors is primarily determined by the capacitor internal temperature. The capacitor lifetime roughly doubles for every 10 °C reduction in internal temperature. SynQor recommends running 100 V rated electrolytic capacitors at 90 V, which dramatically increases hold-up time for a given capacitor volume (see Figure E). A built-in circuit automatically discharges the hold-up capacitor when the input voltage is removed.

Although Equation A has been adjusted to account for approximated losses, factors such as load power, temperature, capacitor ESR, and PCB trace resistance may impact the amount of useable energy delivered by the hold-up capacitor. Additionally, Equation A does not account for capacitor tolerance, which is typically ±20% for aluminum electrolytics.

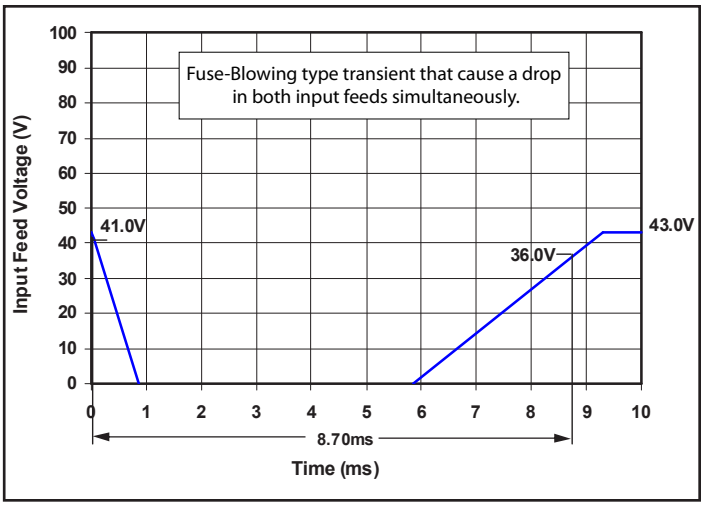


Figure F: *The PICMG 3.0 R2.0 AdvancedTCA Base Specification requires continuous operation through a zero-volt transient, lasting 5 ms (Section 4.1.2.2). However, this is not a square wave: the voltage starts at a minimum amplitude of -43 V, falls at 50 V/ms, remains at 0 V for 5 ms, and then rises at 12.5 V/ms. At the worst case values of the hold-up connect threshold and the management power under-voltage lockout threshold, the required hold-up time is 8.70 ms*

EXTERNAL HOLD-UP TRIM RESISTOR SELECTION

R_{trim} is the external hold-up trim resistance for a given desired nominal hold-up capacitor charge voltage (V_H) (see Figure G):

$$R_{trim} = \left(\frac{500{,}000}{V_H - 50} - 10{,}000\right)\ \Omega \qquad \textit{Equation C}$$

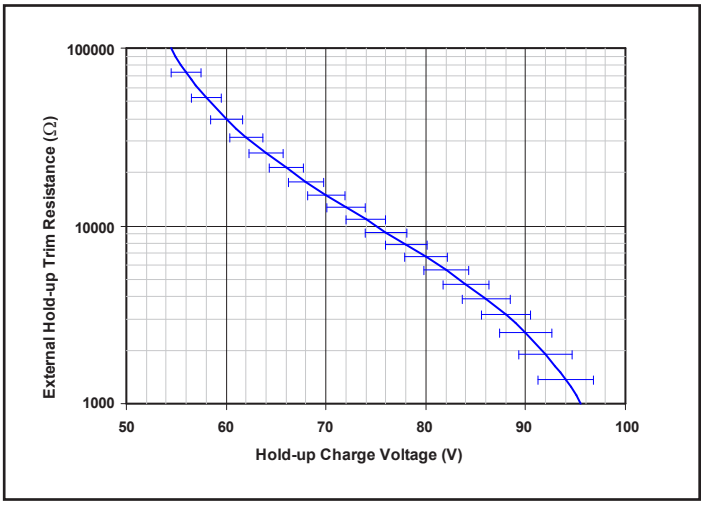


Figure G: *Plot of Equation C, used to choose the external trim resistor value based on the desired Hold-up Capacitor charge voltage. Error bars indicate the worst case range of charge voltage for a given external trim resistor value (assumes 1%, 100 ppm for external trim resistor tolerance). Worst case calculation over temp range -40 °C to 125 °C.*

FULL FEATURE APPLICATION NOTES

I²C Data Reporting Interface: Available on the full feature version of the module, the iQor I²C Serial Interface monitors 5 analog parameters and 6 status bits. The actual analog parameter values are calculated by multiplying by the specified scaling factors (see Table 1). The status bits are interpreted in Table 2. The initial value of all registers is zero. Data in the registers begins updating 300 ms after management power startup, and continues updating at approximately 100 ms intervals during steady-state operation. All registers are updated simulatneously.

I²C Protocol: Reading from any internal register of the iQor monitor requires that an internal (pseudo) register, Data_Pointer, be initialized prior to reading (see Figure I).

Data_Pointer is write-only. It is written from the second byte of any I2C WRITE message (the first byte is the 7 bit I2C Address and the R/W bit). Subsequent data bytes in a WRITE message (3rd Byte and beyond) only increment Data_Pointer.

Any READ message will return the value of the internal register referenced by Data_Pointer and increments Data_Pointer by one. For instance, if the master acknowledges (AK), the next internal register referenced by Data_Pointer will be returned and Data_Pointer will be incremented by one. This process is repeated until the master does not acknowledge (NACK) and issues a STOP bit.

Data_Pointer is an 8bit value. It is initialized to 00h at reset, and after reaching FFh, it will not overflow.

Writing to registers not defined in Table 1 has no effect. Reading from these undefined registers will return 00h. In both cases Data_Pointer is incremented.

Data_ Pointer Value	Parameter	Description	Scaling Factor
1Eh	Status Bits	Digital Signals (see Table 2)	N/A
1Fh	HU_CAP	Voltage between HU_CAP and -48V_OUT	0.398 V/bit
21h	-48V_Current	-48Vout Current	0.094 A/bit
22h	-48V_A	Voltage between VRTN_A and -48V_A	0.325 V/bit
23h	-48V_B	Voltage between VRTN_B and -48V_B	0.325 V/bit
28h	Temperature	Average Unit Temperature	(1.961 °C/bit) – 50 °C

Table 1: *Internal register memory map.*

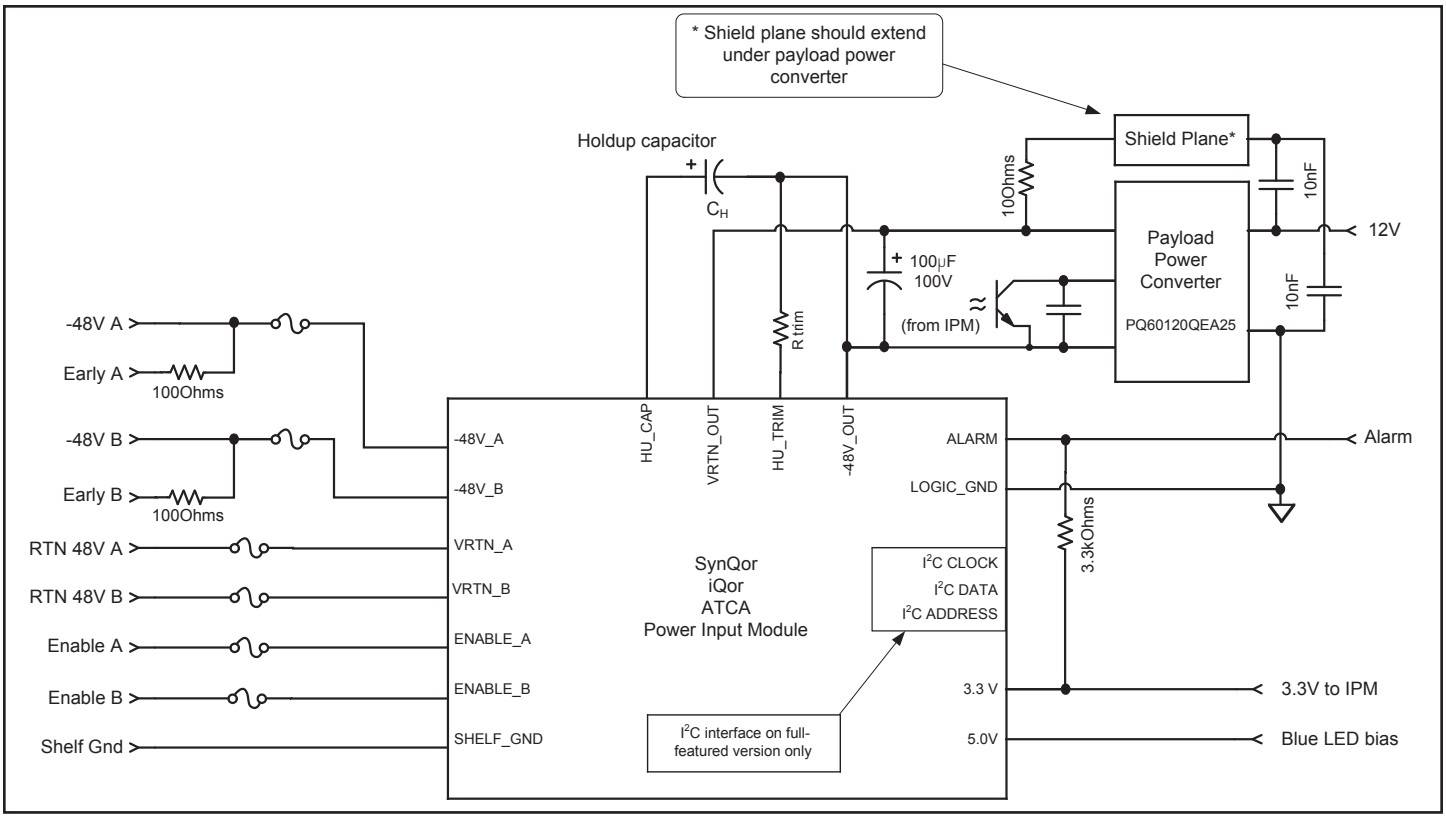


Figure H: *Typical Application Diagram*

Bit	Name	Description	Value	Translation
0	ENABLE_A	Enable A Signal State	0	EN_A is Disabled
			1	EN_A is Enabled
1	ENABLE_B	Enable B Signal State	0	EN_B is Disabled
			1	EN_B is Enabled
2	ALARM	Alarm Signal State	0	Primary side Alarm is not SET
			1	Primary side Alarm is SET
3	N/A	Reserved		
4	HOLDUP	Holdup Switch State	0	Holdup Cap is not connected to -48V Out
			1	Holdup Cap is connected to -48Vout
5	HOTSWAP	Hotswap Switch State	0	Hotswap switch is OFF
			1	Hotswap switch is ON
6	VOUT_ LOW	-48Vout Under-Voltage Alarm	0	Vout is below threshold
			1	Vout is above threshold
7	N/A	Reserved		

Table 2: *The status byte represents 6 different digital signals and their digital state. Note: 1) Bit0 ⇒ LSb, Bit7 ⇒ MSb*

I²C Protocol: Reading from any internal register of the iQor monitor requires that an internal (pseudo) register, Data_Pointer, be initialized prior to reading (see Figure I).

Data_Pointer is write-only. It is written from the second byte of any I²C WRITE message (the first byte is the 7 bit I²C Address and the R/W bit). Subsequent data bytes in a WRITE message (3rd Byte and beyond) only increment Data_Pointer.

Any READ message will return the value of the internal register referenced by Data_Pointer and increments Data_Pointer by one. For instance, if the master acknowledges (AK), the next internal register referenced by Data_Pointer will be returned and Data_Pointer will be incremented by one. This process is repeated until the master does not acknowledge (NACK) and issues a STOP bit.

Data_Pointer is an 8bit value. It is initialized to 00h at reset, and after reaching FFh, it will not overflow.

Writing to registers not defined in Table 1 has no effect. Reading from these undefined registers will return 00h. In both cases Data_Pointer is incremented.

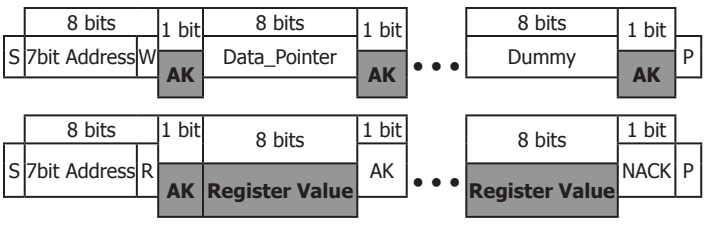


Figure I: *Typical I²C read transmission. Note: S = START, W = WRITE, R = READ, AK = acknowledged, NACK = NOT acknowledged, P = STOP. Clear boxes originate in the I2C Master and shaded boxes originate in the I²C Slave.*

Example from the point of view of the I²C Master:

1) START transmission.
2) Send 56h (addresses unit for writing, given address 56h was selected as shown in Table 4).
3) Send 22h (loads 22h into Data_Pointer).
4) STOP transmission.
5) START next transmission.
6) Send 57h (addresses unit for reading).
7) Unit will respond with the value of -48V_A (register 22h as shown in Table 1).
8) ACK (Data_Pointer is automatically incremented to 23h).
9) Unit will respond with the value of -48V_B (register 23h).
10) NACK.
11) Stop Transmission.

I²C Address structure:

7 bit I²C Address + R/W bit

Four bits are fixed (0101), three bits (xyz) are variable, and the least-significant bit is the read/write bit.

8 bit I²C Address		
0 1 0 1	x y z *	R/W

Table 3: *I²C address structure.*

I²C Address selection: The three bits (xyz) of the I²C Address are set with a single external resistor from the I2C_ADR (pin 10) to LOGIC_GND (pin 13). The 8 possible addresses are shown in Table 4 with the respective resistance values.

External programming resistances for I²C Address Selection		
I²C address for write (R/W = 0)	xyz from Table 3	R (Ω)
5Eh	111	Open
5Ch	110	100000
5Ah	101	40200
58h	100	20000
56h	11	10000
54h	10	4020
52h	1	2000
50h	0	Short

Table 4: *I²C address selection.*

PCB layout

Connections to the address selection resistor must follow the Kelvin method to minimize effects of DC offsets and ripple/noise present in the general GND. The interconnection between Digital GND and Power GND or GND plane should also be in such a way that noise is not coupled to the address selection circuitry. See Figure J

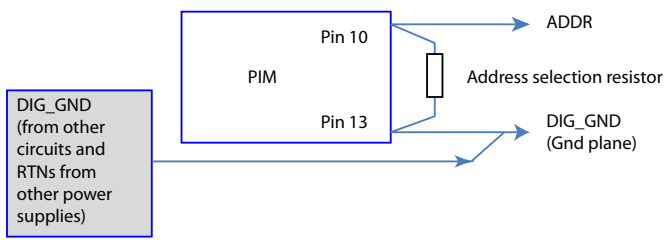
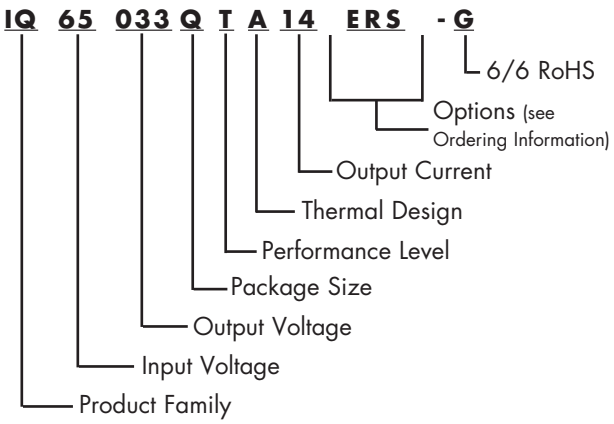


Figure J: *Resistor Diagram*

PART NUMBERING SYSTEM

The part numbering system for SynQor's dc-dc converters follows the format shown in the example below.



The first 12 characters comprise the base part number and the last 3 characters indicate available options. The "-G" suffix indicates 6/6 RoHS compliance.

Application Notes

A variety of application notes and technical white papers can be downloaded in pdf format from our website.

RoHS Compliance: The EU led RoHS (Restriction of Hazardous Substances) Directive bans the use of Lead, Cadmium, Hexavalent Chromium, Mercury, Polybrominated Biphenyls (PBB), and Polybrominated Diphenyl Ether (PBDE) in Electrical and Electronic Equipment. This SynQor product is 6/6 RoHS compliant. For more information please refer to SynQor's RoHS addendum available at our RoHS Compliance / Lead Free Initiative web page or e-mail us at rohs@synqor.com.

ORDERING INFORMATION

The tables below show the valid model numbers and ordering options for converters in this product family. When ordering SynQor converters, please ensure that you use the complete 15 character part number consisting of the 12 character base part number and the additional 3 characters for options. Add "-G" to the model number for 6/6 RoHS compliance.

Model Number	Input Voltage	MGMT Power	Max Output Current
IQ65033QTA14xyz-G	36-75 V	3.3V & 5.0V	14 A

The following options must be included in place of the ***w x y z*** spaces in the model numbers listed above.

Options Description: x y z		
Threshold Protocols	**Pin Style**	**Feature Set**
E - Extended Input Threshold Protocol (ETSI)	K - 0.110" N - 0.145" R - 0.180" Y - 0.250"	S - Standard F - Full-Feature (I^2C)

Not all combinations make valid part numbers, please contact SynQor for availability.

Contact SynQor for further information and to order:

Phone:	978-849-0600
Toll Free:	888-567-9596
Fax:	978-849-0602
E-mail:	power@synqor.com
Web:	www.synqor.com
Address:	155 Swanson Road Boxborough, MA 01719 USA

PATENTS

SynQor holds numerous U.S. patents, one or more of which apply to most of its power conversion products. Any that apply to the product(s) listed in this document are identified by markings on the product(s) or on internal components of the product(s) in accordance with U.S. patent laws. SynQor's patents include the following:

5,999,417	6,222,742	6,545,890	6,594,159	6,894,468	6,896,526
6,927,987	7,050,309	7,072,190	7,085,146	7,119,524	7,269,034
7,272,021	7,272,023	7,558,083	7,564,702	7,765,687	7,787,261
8,023,290	8,149,597	8,493,751	8,644,027	9,143,042	

WARRANTY

SynQor offers a three (3) year limited warranty. Complete warranty information is listed on our website or is available upon request from SynQor.